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(56) Documents Cited

US 5266831 A US 4707720 A

(58) Field of Search

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(54) Abstract Title

A gated semiconductor device having a field plate termination

(57) A gated semiconductor device, such as a MOSFET or IGBT, having a field plate termination structure which is connected to the gate electrode by multiple n-p junctions defining a semiconductor breakdown diode is disclosed. The device comprises a source 4, source electrode 10, insulating layer 8, gate electrode 7b, n-p junction 15, extended gate electrode forming the field plate 11, metal connection 13, equipotential ring 14 and channel stop 5. An alternative structure is also disclosed.

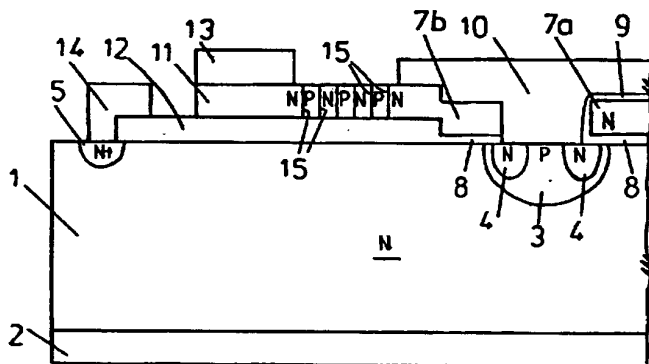


FIG. 2

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1-3

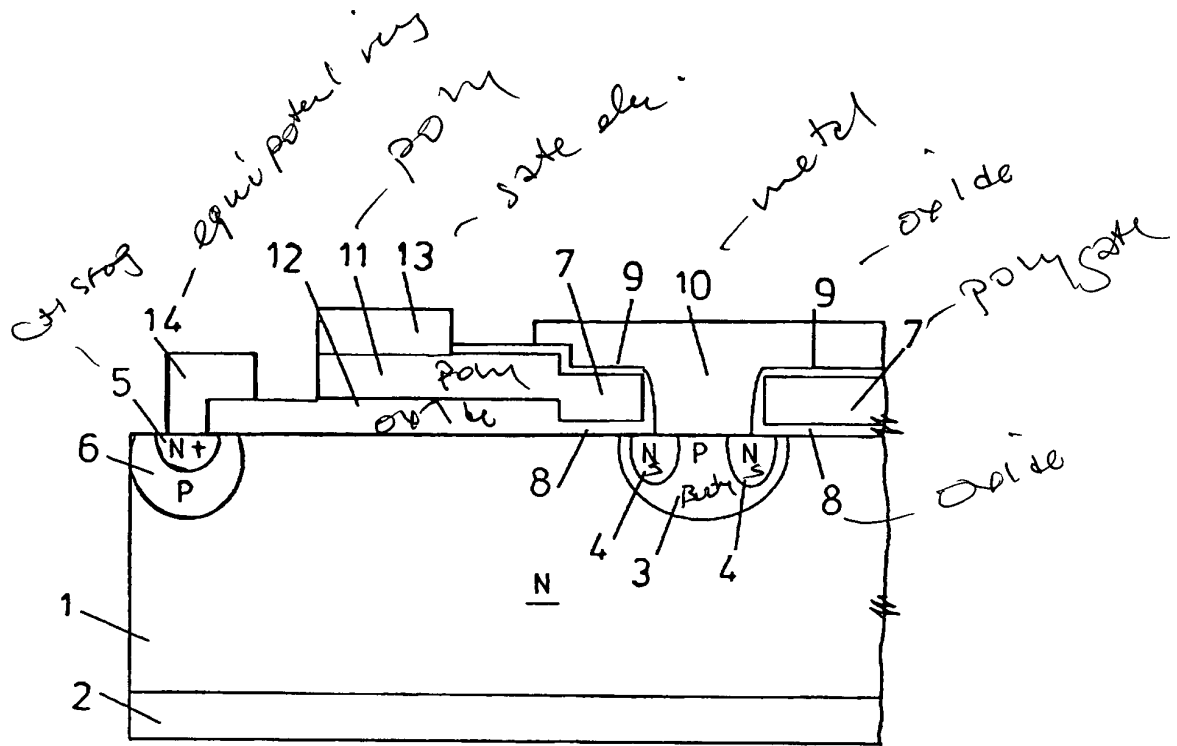


FIG. 1

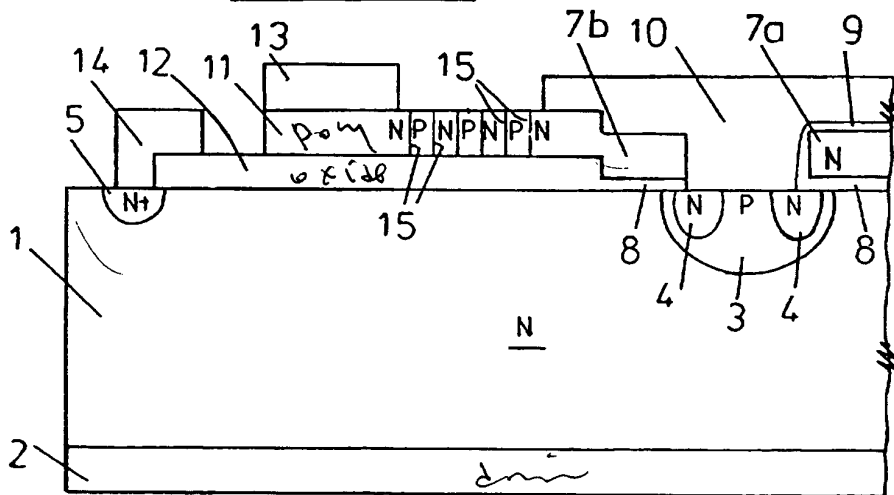


FIG. 2

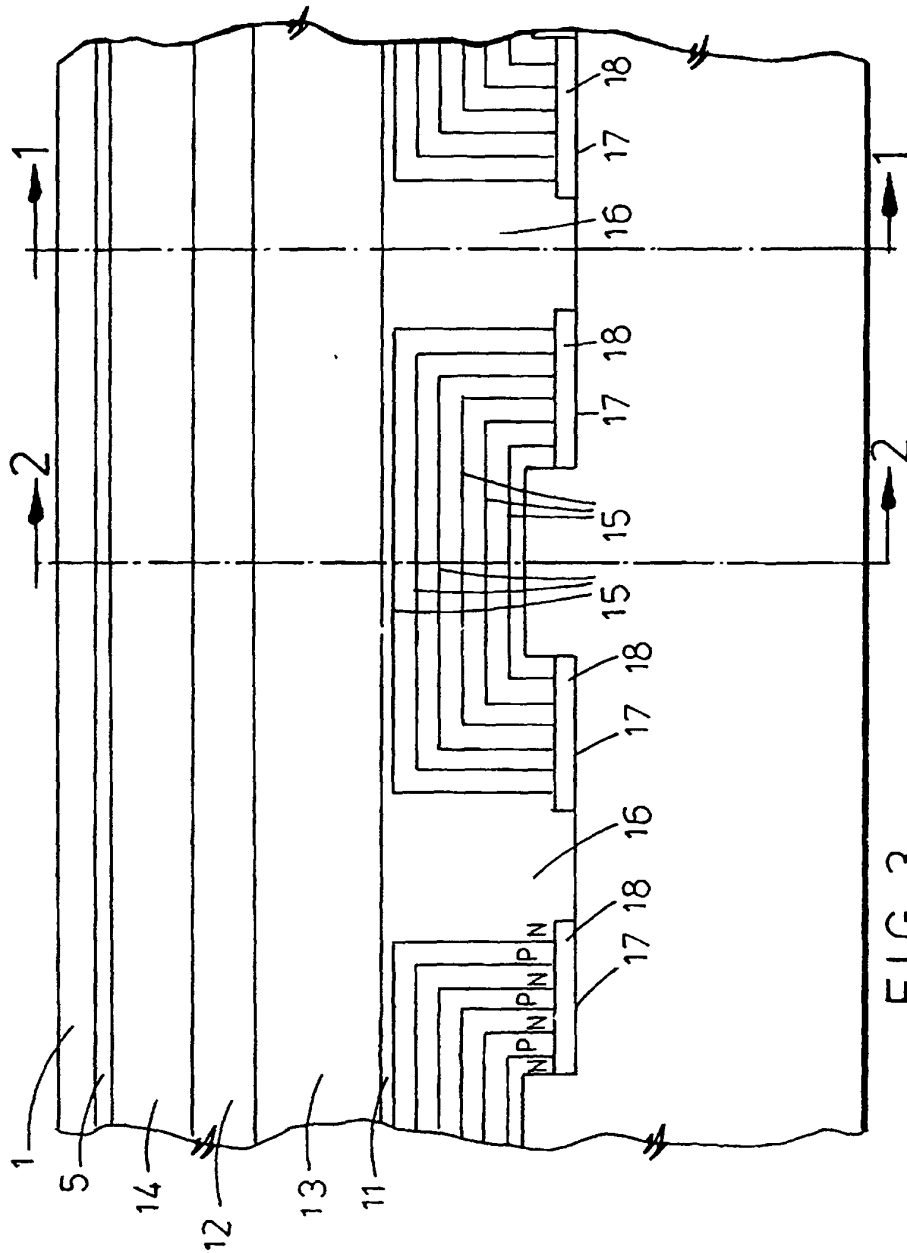


FIG. 3

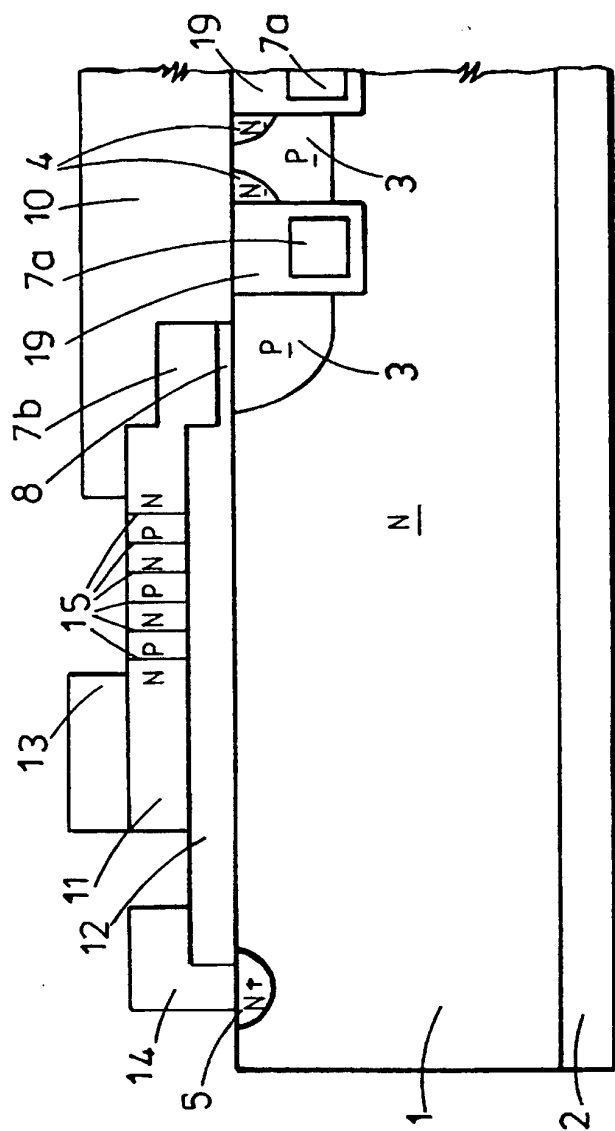


FIG. 4

GATED SEMICONDUCTOR DEVICE

The present invention relates to a gated semiconductor device having a field plate termination.

For MOS gated semiconductor devices such as field effect transistors, the standard method of termination is to continue source metal beyond the periphery of an active area of the device so as to form a field plate extending around the periphery of the device. In an N-channel MOSFET, when a positive bias is applied to the drain whilst the gate and source are connected to the ground potential the transistor is in the forward-biased off state. This creates a depletion region which is brought to the surface more gradually at the edge of the device than at the centre due to the presence of the field plate formed from the continuation of the source metal. This reduces the peak electric field at the periphery of the device, thus increasing the breakdown voltage.

One requirement of a MOSFET device is to connect the gate to a gate bond pad. The gate is normally made of polysilicon which has a significant resistance that combines with the device capacitance to create a time constant RC. In order to give acceptable switching characteristics it is thus necessary to break the source metal by distributing metal gate electrodes throughout the structure and/or around the periphery of the device. Some MOSFETs use a striped rather than a matrix polysilicon design, in which case the gate electrode may also be needed to connect the polysilicon gate stripes together. The larger the gate electrode area, the faster the switching, but also the higher the on resistance, and so there needs to be a trade-off between speed and resistance.

It is known to combine the functions of a field plate and a gate electrode by forming a conductive layer separated from the substrate by an insulating layer and extending around the active surface area between the field plate and gates which are positioned around the periphery of the active area. In this type of arrangement, the conductive layer and the peripheral gates may be formed from portions of a single layer of polysilicon on which a field plate conductor is deposited.

These known devices in which the field plate and peripheral gates are interconnected can be damaged or destroyed however by electrostatic discharge or circuit transients. An electrostatic discharge (e.g. from a human being) can charge up the gate to a potential beyond its rupture voltage, thus destroying or irreparably damaging the insulating layer which separates the gate from the substrate.

It is an object of the present invention to provide a gated semiconductor device which obviates or mitigates the above disadvantage.

According to the present invention, there is provided a gated semiconductor device comprising a substrate defining an active surface area including at least one source region, at least one gate formed adjacent to and insulated from the at least one source region, a source electrode in electrical contact with the source region, and a termination extending around the periphery of the active surface area, the termination comprising a gate electrode and a layer of conductive material electrically connected between the gate electrode and the said at least one gate, wherein the layer of conductive material is in electrical contact with the source electrode and incorporates at least one N-P junction defining a semiconductor breakdown diode located so as to be connected in series between the gate electrode and the source electrode.

Preferably, spaced apart portions of an outer edge of the source electrode electrically contact the conductive layer, openings are formed in the conductive layer spaced apart around the outer edge of the source electrode such that each said spaced apart portion of the source electrode edge is located between the openings of a respective pair of openings, and N-P junctions are formed in the conductive layer outside the outer edge of the source electrode such that each junction extends between and terminates at the openings of a respective one of the said pairs of openings.

The layer of conductive material and the or each gate to which the conductive material is connected may be formed from a single layer of polysilicon. The polysilicon layer may support a metal gate electrode. The polysilicon layer is preferably connected to a plurality of gates distributed adjacent the periphery of the active surface area of the substrate. Preferably a plurality of diodes are arranged in

series between the gate electrode and the source electrode, the diodes being formed from successive sections of N and P type conductive materials.

An embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a schematic representation of one edge of a conventional gated semiconductor device;

Figure 2 is a schematic representation of one edge of a gated semiconductor device in accordance with the present invention;

Figure 3 is a plan view of the device edge shown in Figure 2; and

Figure 4 is a view similar to that of Figure 2 showing a trench MOSFET structure in accordance with the present invention.

Referring to Figure 1, there is illustrated a prior art gated semiconductor device, in this instance an N-channel MOSFET, comprising a substrate 1 on which is formed a drain 2. Diffused into the substrate 1 are areas of differing conductivity forming body regions 3, source regions 4, and a channel stop region formed by floating N region 5 within P region 6 which extends around the periphery of the substrate, and thus around an active device area in which the regions 3 and 4 are formed. Alternatively, the channel stop region may be formed from just an N region 5, or may be omitted altogether. Polysilicon gate electrodes 7 are provided on layers of insulator 8 defined by an oxide layer and are covered by further layers of insulator 9. A metal source layer 10 contacts regions 3 and 4 and extends over part of the peripheral insulator layer 9.

A polysilicon layer 11 extends radially outwards from the gate 7 which is adjacent the edge of the device. The polysilicon layer 11 is formed on an oxide layer 12 which may be thicker than the oxide layer 8 beneath the gate 7 so as to improve the breakdown voltage in some embodiments (e.g. higher voltage variants) although this is not essential. A conductive gate electrode 13 is formed on the polysilicon layer 11, and a conductive equipotential ring 14 contacts the optional channel stop region 5, 6.

In use, when a positive bias is applied to drain 2 whilst the gates 7 and source 10 are connected to ground potential, the transistor is in the forward biased off state.

The forward potential is supported across the P-body 3 and N-drain region 1. This creates a depletion region which is brought to the surface more gradually at the edge of the device by the polysilicon layer 11. This reduces the peak electric field at the periphery of the device, increasing the breakdown voltage.

As the polysilicon layer 11 is connected to the gate electrode 13 a very effective structure is formed which distributes gate current around the periphery of the active area. The combination of the gate electrode 13 and polysilicon layer 11 can still function as a field plate because during the forward biased on state both the gates 7 and source 10 are at ground potential. Gate electrode 13 could also be combined with conventional gate electrodes (not shown) feeding central regions of the device and is connected remotely to a gate bond pad (not shown in Figure 1).

Referring to Figure 2, there is illustrated a device according to the present invention. The same reference numerals are used where appropriate as are used in Figure 1. The device comprises a drain 2, body region 3, source regions 4 and optional channel stop region 5. Gate 7a is insulated from the substrate 1 by insulator 8. Region 7b, which corresponds in position to the peripheral gate 7 of the arrangement of Figure 1, is shorted to the source electrode 10 and therefore does not function as a gate in the arrangement of Figure 2. A gate electrode 13 is provided on the polysilicon layer 11 which is located on oxide insulating layer 12. An equipotential ring 14 is provided around the periphery of the device.

A gate-source zener diode suitable for electrostatic discharge (ESD) protection, circuit transient protection etc is provided in the polysilicon layer by introducing dopants so as to define alternate N and P regions between which junctions 15 are formed in the polysilicon layer 11. The junctions 15 form a series of alternately forward and reverse biased zener diodes between the source electrode 10 and the gate electrode 13. Each diode typically has a low breakdown voltage (V_z), e.g. 5V but in combination a larger overall V_z can be achieved as the individual diode breakdown voltages in effect are summed together. Combinations of diodes have the further advantage that the overall V_z can be made the same in both directions.

Figure 3 is a plan view of Figure 2, the position of the section represented by Figure 2 being indicated in Figure 3 by line 2-2. It will be seen that the N and P doped regions are C-shaped such that regions 16 of the polysilicon layer 11 are defined between regions of the polysilicon layer 11 occupied by the junctions 15. The regions 16 extend beneath but are insulated from the source metal layer 10 and provide a gate current path to peripheral gates (not shown) which underlie and are insulated from the source electrode 10. The ends of the C-shaped N and P doped regions are spaced from the peripheral regions 7b (Figure 2) which underlie the source metal 10 (the edge of which is indicated by lines 17) by openings 18 formed in the polysilicon layer 11. Thus spaced apart portions of the outer edge of the source electrode electrically contact the conductive layer 11 between respective pairs of the openings 18 but those spaced apart portions are located on the opposite side of the junctions 15 from the gate electrode 13. Accordingly current can flow directly between the gate and source electrodes only if the diode junctions break down. Gate current in contrast flows beneath the source electrode 10 through the regions 16 which are located between the regions of the conductive layer 11 in which the junctions 15 are formed.

In the illustrated example, the peripheral gates and the gate current path regions 16 are N doped. However, the peripheral gates and the gate current path regions may be P doped. Similarly, the polysilicon which contacts the source metal is shown N doped but could be P doped. The various possible combinations may require different numbers of junctions 15 to achieve required diode characteristics.

In Figure 3, a section on the line 1-1 would reveal a structure similar to the conventional structure illustrated in Figure 1, the only difference being the optional addition of the P-region 6. It will of course be appreciated that alternative layouts to that illustrated in Figures 2 and 3 are possible in order to establish breakdown diodes connected in series between the gate and source electrodes.

Preferably the N and P rings which define the junctions 15 are formed by using a body implant to dope the polysilicon such that it becomes P type at the same time as creating the body regions 3. The rings may then be patterned (e.g. with a

resist mask covering where the P type rings are required) prior to a source implant or deposition. This source implant or deposition would then dope the exposed polysilicon so as to become N type at the same time as creating the source regions 4.

An advantage of this process is that by selectively blocking out the source the channel stop 5 can be made N type rather than a floating N within a P type body region as in Figure 1. A floating channel stop can cause difficulties during dynamic breakdown conditions. The ability to selectively pattern the source diffusion is also a requirement of many intelligent MOSFET production processes.

Alternatively, the polysilicon layer 11 may be doped P type in a separate stage after the polysilicon deposition but before polysilicon patterning to a concentration higher than any anticipated body dope. This additional step makes it possible to trim the device characteristics (e.g. the threshold voltage) by altering the body implant without affecting the V_z of the ESD protection diodes.

The thick insulating layer 12 which underlies the gate electrode 13 and outer portions of the conductive layer 11 may be omitted so that the polysilicon layer 11 is only insulated by a thin layer of oxide in the same fashion as the gates 7a.

The field plate structure as described could also be combined with other termination techniques such as SIPOS and floating rings. Although it has been particularly described with relation to an N-channel MOSFET, it should be appreciated that the invention is applicable to N- and P-channel gated devices. MOSFETs and IGBTs are the most common MOS gated devices, although several other types also exist.

Referring now to Figure 4, this illustrates an embodiment of the invention which incorporates trench MOSFET structures rather than the planar MOSFET structures of Figures 2 and 3. The same reference numerals are used in Figure 4 as in Figure 2 where appropriate. The structure of Figure 4 differs from that of Figure 2 in that gate electrodes 7a are formed within trenches which penetrate the body region 3 and are located adjacent the source regions 4. The gates 7a are insulated from the surrounding structure by a body 19 of insulating material which fills the trench. It will be appreciated that the gate electrode 7a will be connected to the gate electrode

field plate 13 by portions of a polysilicon layer 11 which extend beneath and are insulated from the source electrode 10. Thus gate current can flow between the gate electrode 13 and the gate 7a but the diode junctions 15 prevent gate current being shorted to the source electrode 10 unless the voltage between the two is sufficient to break down the diode junctions 15.

CLAIMS

1. A gated semiconductor device comprising a substrate defining an active surface area including at least one source region, at least one gate formed adjacent to and insulated from the at least one source region, a source electrode in electrical contact with the source region, and a termination extending around the periphery of the active surface area, the termination comprising a gate electrode and a layer of conductive material electrically connected between the gate electrode and the said at least one gate, wherein the layer of conductive material is in electrical contact with the source electrode and incorporates at least one N-P junction defining a semiconductor breakdown diode located so as to be connected in series between the gate electrode and the source electrode.

2. A device according to claim 1, wherein spaced apart portions of an outer edge of the source electrode electrically contact the conductive layer, openings are formed in the conductive layer spaced apart around the outer edge of the source electrode such that each said spaced apart portion of the source electrode edge is located between the openings of a respective pair of openings, and N-P junctions are formed in the conductive layer outside the outer edge of the source electrode such that each junction extends between and terminates at the openings of a respective one of the said pairs of openings.

3. A device according to claim 1 or 2, wherein the layer of conductive material and the said at least one gate are formed from a single layer of polysilicon.

4. A device according to claim 3, wherein the gate electrode is of metal and is supported by the polysilicon layer.

5. A device according to any preceding claim, wherein the layer of conductive material is connected to a plurality of gates distributed adjacent the periphery of the active surface area of the substrate.
6. A device according to any preceding claim, comprising a plurality of diodes arranged in series between the gate electrode and the source electrode, the diodes being formed by successive sections of N and P type conductive material.
7. A device according to any preceding claim, wherein the conductive layer is formed on an oxide layer which extends beneath the at least one gate.
8. A device according to claim 7, wherein the oxide layer beneath the conductive layer is thicker than the oxide layer beneath the gate.
9. A gated semiconductor device substantially as hereinbefore described with reference to Figures 2 and 3 or Figure 4 of the accompanying drawings.



Application No: GB 9919285.8
Claims searched: 1-9

Examiner: Emma Rendle
Date of search: 24 November 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:
UK CI (Ed.Q): H1K (KCAL, KCAX, KCBS, KDEG, KGAGX, KKAG, KKAX)
Int CI (Ed.6): H01L 29/06, 29/73
Other: EPOQUE: WPI, EPODOC, PAJ

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	US 4 707 720 (TOKYO SHIBAURA ELECTRIC) see whole document, especially Figures 17 and 18.	1, 2, 6, 7, 8
A	US 5 266 831 (MOTOROLA) see whole document.	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.